# Precision RTL

## Precision RTL is Mentor Graphics' entry-level FPGA synthesis solution offering excellent quality of results and part of Mentor Graphics' comprehensive FPGA vendor independent solution.

With a rich feature set that includes advanced optimizations, award-winning analysis, and industry-leading language support, Precision RTL enables vendor-independent design, accelerates time to market, eliminates design defects, and delivers superior quality of results.

## Key Features and Benefits

**FPGA Vendor Independent Synthesis**

- Support for Actel, Altera, Lattice, and Xilinx
- OEM support for Abound Logic, Achronix, Atmel, QuickLogic, and TierLogic
- Same HDL and constraints for all devices

**Excellent Quality of Results**

- Meet performance and area goals quickly
- Advanced timing-driven optimizations
- Technology inference for multiple vendors

**Award-Winning-Analysis**

- RTL and gate-level technology schematics
- Interactive static-timing engine to perform"what-if" timing analysis

**Industry Leading Language Support**

- Supports any combination of Verilog, VHDL, SystemVerilog, and EDIF formats
- Supports Synopsys Design Constraints

**Precise-IP™**

- Generate building block IP for any device
- Leverage 3rd party IP validated for Precision

**Integration with Mentor Tools**

- Design Reuse with HDL Designer™

- Equivalence Checking with FormalPro™

**ASIC Prototyping Support**

- Eases ASIC-to-FPGA migration
- Automatic gated clock conversion
- Conversion of DesignWare instances
- Support for ASIC timing constraints (SDC)