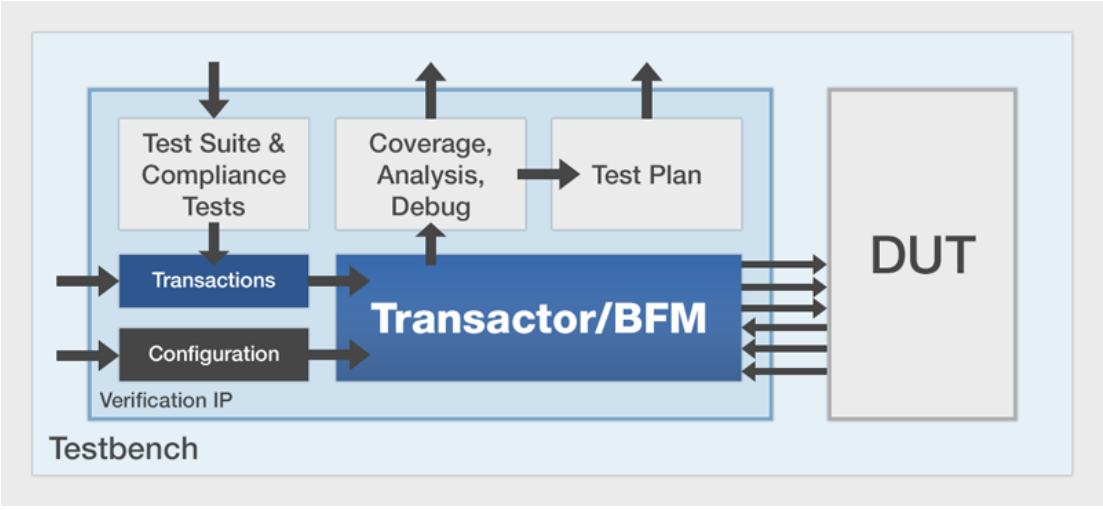
Verification IP

Comprehensive verification IP built using advanced methodologies for fastest time to verification sign-off.

Today's designs rely heavily on a growing variety of complex industry standard interfaces that must be verified to ensure IP interoperability and system behavior. Mentor's verification IP (VIP) improves quality and reduces schedule times by building Mentor’s protocol and methodology expertise into a library of reusable components that support many industry standard interfaces. This frees up engineering resources from having to spend time developing BFMs, verification components, or VIP themselves, enabling them to focus on the unique and high-value aspects of their design.

Mentor's VIP integrates seamlessly into advanced verification environments, including testbenches built using UVM, Verilog, VHDL, and SystemC. It is the industry's only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility.

Combined with the Questa Verification Platform, complete VIP components reduce bring up time and enable rapid coverage closure. Comprehensive protocol assertions allow Questa Formal users to exhaustively prove design correctness, while support for Veloce Emulation Systems enables users to easily transition to high-performance simulation acceleration for orders-of-magnitude gains in throughput.



Features and Highlights

- Comprehensive test suite & compliance tests
- Complete protocol coverage and checking

- Native SystemVerilog UVM tests and components
- SystemVerilog, Verilog, VHDL, and SystemC testbench support
- Support for simulation, acceleration, and formal verification environments
- Integrated support for verification planning and management
- Transaction-level scoreboarding, analysis, and debug
- Synthesizable memory models for use with simulation acceleration and emulation